**BUS SYSTEM USING MULTIPLEXER**

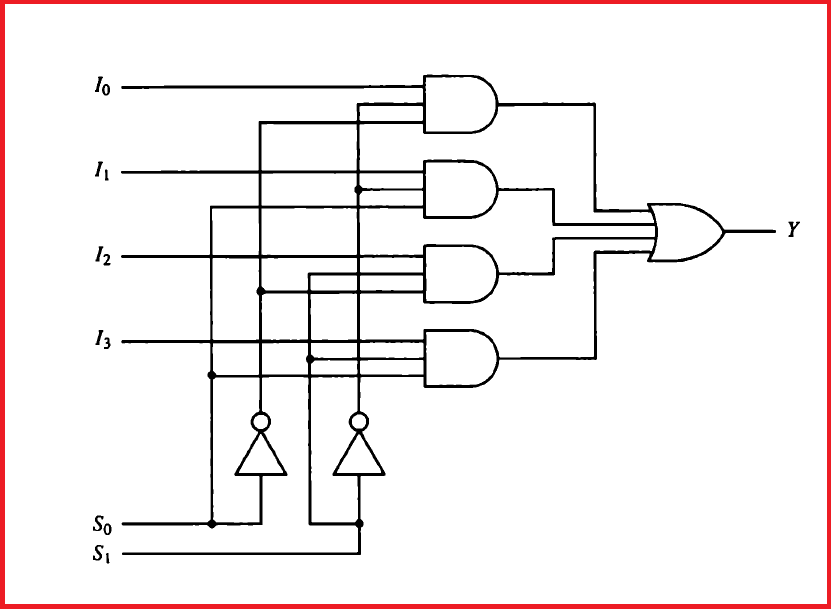
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**MULTIPLEXER(MUX)**

A multiplexer is a combinational circuit that receives binary information from one of 2n input data lines and directs it to a single output line. The selection of a particular input data line for the output is determined by a set of selection inputs. A 2n -to-1 multiplexer has 2n input data lines and n-input selection lines whose bit combinations determine which input data are selected for the output.

A 4-to-1-line multiplexer is shown in figure 1. Each of the four data inputs I0 through I3 is applied to one input of an AND gate. The two selection inputs S1 and S0 are decoded to select a particular AND gate. The outputs of the AND gates are applied to a single OR gate to provide the single output. To demonstrate the circuit operation, consider the case when S1S0 = 10. The AND gate associated with input I2 hastwo of its inputs equal to 1. The third input of the gate is connected to I2.The other three AND gates have at least one input equal to 0, which makes their outputs equal to 0. The OR gate output is now equal to the value of I2, thus providing a path from the selected input to the output. The 4-to-1 line multiplexer of figure has six inputs and one output. A truth table describing the circuit needs 64 rows since 6-input variables can have 26 binary combinations. This is an excessively long table and will not be shown here. A more convenient way to describe the operation of multiplexers is by means of a function table. The function table for the multiplexer is shown in Table 1. The table demonstrates the relationship between the four data inputs and the single output as a function of the selection inputs S1 and S0.



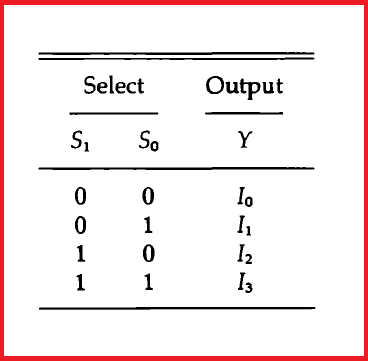
**Figure 1:** 4-to-1-line multiplexer

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When the selection inputs are equal to 00, output Y is equal to input I0. When the selection inputs are equal to 01, input I1 has a path to output Y, and similarly for the other two combinations. The multiplexer is also called a data selector, since it selects one of many data inputs and steers the binary information to the output.

**Table 1: Function Table for 4-to-1 Line Multiplexer**



The AND gates and inverters in the multiplexer resemble a decoder circuit, and indeed they decode the input selection lines. In general, a *2n-to-1*-line multiplexer is constructed from an *n-to-2n* decoder by adding to it *2n*input lines, one from each data input. The size of the multiplexer is specified by the number *2n* of its data inputs and the single output. It is then implied that it also contains *n-*input selection lines.

As in decoders, multiplexers may have an enable input to control the operation of the unit. When the enable input is in the inactive state, the outputs are disabled, and when it is in the active state, the circuit functions as a normal multiplexer. The enable input is useful for expanding two or more multiplexers to a multiplexer with a larger number of inputs.

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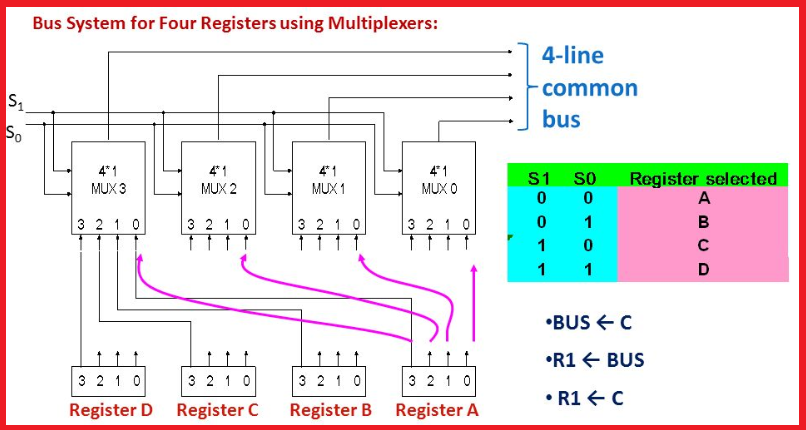
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A typical digital computer has many registers, and paths must be provided to transfer information from one register to another. The number of wires will be excessive if separate lines are used between each register and all other registers in the system. A more efficient scheme for transferring information between registers in a multiple-register configuration is a **common bus system**.

**A bus structure** consists of a set of common lines, one for each bit of a register, through which binary information is transferred one at a time. Control signals determine which register is selected by the bus during each particular register transfer.

One way of constructing **a common bus system is with multiplexers**. The multiplexers select the source register whose binary information is then placed on the bus. The construction of a bus system for four registers in shown in figure 2.



**Figure 2: Bus System for Four Registers**

Each register has four bits, numbered 0 through 3. The bus consists of four 4X1 multiplexers each having four data inputs, 0 through 3, and two selection inputs, S1 and S0. In order not to complicate the diagram with 16 lines crossing each other, we use labels to show the connections from the outputs of the registers to the inputs of the multiplexers. For example, output 1 of register A is connected to input 0 of Mux 1 because this input is labelled A1. The diagram shows that the bits in the same significant position in each register are connected to the data inputs of one multiplexer to form one line of the bus. The MUX 0 multiplexes the four 0 bits of the registers, MUX 1 multiplexes the four 1 bits of the registers, and similarly for the other two bits.

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The two selection lines S1 and S0 are connected to the selection inputs of all four multiplexers. The selection lines choose the four bits of one register and transfer them into the four-line common bus. When S1S0=00, the 0 data inputs of all four multiplexers are selected and applied to the outputs that form the bus. This causes the bus lines to receive the content of register A since the outputs of this register are connected to the 0 data inputs of the multiplexers. Similarly, register B is selected if S1S0=01, and so on. Table shown in above figure shows the register that is selected by the bus for each of the four possible binary value of the selection lines.

In general, a bus system will multiplex *k* registers of *n* bits each to produce an *n-*line common bus. The number of multiplexers needed to construct the bus is equal to n, the number of bits in each register. The size of each multiplexer must be *k X 1* since it multiplexes *k* data lines.

For example, a common bus for 8- registers of 16 bits each requires 16 multiplexers, one for each line in the bus. Each multiplexer must have eight data input lines and three selection lines to multiplex one significant bit in the eight registers.

The transfer of information from a bus into one of many destination registers can be accomplished by connecting the bus lines to the inputs of all destination registers and activating the load control of the particular destination register selected. The symbolic statement for a bus transfer may mention the bus or its presence may be implied in the statement. The statements are mentioned in above figure.